28th IEEE Workshop on Signal and Power Integrity

May 12-15, 2024 -- Lisbon, PORTUGAL

FINAL PROGRAM

May 12, Sunday

Time	Event
14:00-14:50	Registration
14:50-15:00	Tutorials Welcome
15:00-16:00	TUTORIAL (Part 1) — Lorenzo Codecasa — *Thermal Modeling of Electronic Components and Packages*
16:00-16:30	*Coffee-Break*
16:30-17:30	TUTORIAL (Part 2) — Lorenzo Codecasa — *Thermal Modeling of Electronic Components and Packages*
18:00 onwards	Welcome Reception

May 13, Monday

Time	Session	Event
09:00-09:30		Registration
09:30-09:50		Opening Session
09:50-10:30		KEYNOTE — Rajen Murugan — *Multiphysics and Multidomain Modeling of Semiconductor IC Packaging and Systems*
10:30-11:00		*Coffee-Break*
11:00-11:20	SESSION 1 — Power distribution networks — Chair: Heidi Barnes	Judy Amanor-Boadu — *Leveraging SIMPLIS to Better Predict Server Platform Power Delivery Performance*
11:20-11:40		Morten Schierholz — *PCB based Power Deliver Network Analysis Using Transfer Learning and Artificial Neural Networks*
11:40-12:00		Youcef Hassab — *Application of Gaussian Process Regression for Data Efficient Prediction of PCB-based Power Delivery Network Impedance Features*
12:00-12:20		Tommaso Bradde — *Fast Prediction of Worst-Case Voltage Droops in Power Distribution Networks*
12:20-12:30		SPONSOR PITCH — Victor Medina — *Rohde & Schwarz*
12:30-14:00		*Lunch*
14:00-14:40		KEYNOTE — Cian Ó Mathúna — *MagIC – Making Magnetics Disappear onto Silicon Enabling Power Supply on Chip (PwrSoC) and Power Supply in Package (PwrSiP)*
14:40-15:00	SESSION 2 — Models and methods for SI/PI analysis — Chair: Jose Schutt-Aine	Tim Pattyn — *Differential Interconnects with Integrated Equalization and Common-Mode Filtering for Broadband Signal Integrity Enhancement in High-Speed PAM-4 Signaling*
15:00-15:20		Marco Occhiali — *Impact of Port Type in S-Parameter Extraction of Package and PCB High-Speed Interconnections*
15:20-15:40		Giulia Di Capua — *Models and Methods for the Analysis of PCB Crosstalk in Switch-Mode Power Supplies*
15:40-15:50		Kemal Aygün — *Activity of the IEEE EDMS Technical Committee*
15:50-16:50		POSTER SESSION — Chairs: Antonio Maffucci and Stefano Grivet-Talocia — *& Coffee-Break*
17:00 onwards		City Tour

May 14, Tuesday

Time	Session	Event
09:00-09:40		KEYNOTE — Kemal Aygün — *Solving the Challenges of High-Speed/High-Bandwidth Interconnects for Future System-in-Packages*
09:40-10:00	SESSION 3 — Electro-thermal modeling — Chair: Joana Catarina Mendes	Sarah Sibilia — *Electro-thermal Response of Industrial-grade Graphene for Electronic Packages Applications*
10:00-10:20		Lorenzo Codecasa — *Fast Error-Bounded MOR-based Approximation of Heat Conduction Problems in Electronics*
10:20-10:50		*Coffee-Break*
10:50-11:10	SESSION 4 — AI-based approaches for SI/PI analysis — Chair: Kemal Aygün	Riccardo Trinchero — *Modeling of IC Buffers from Channel Responses via Machine Learning Kernel Regression*
11:10-11:30		Jan Krummenauer — *Evaluating Deep Reinforcement Learning for Macromodel Synthesis*
11:30-11:50		Markus Stiemer — *Dimensional Reduction by Auto-Encoders in Machine Learning Based Power Integrity Analysis*
11:50-12:10		Yutaka Uematsu — *Abnormal-state-clustering for In-vehicle Cable Communication using Equalizer Parameters and Machine Learning Approach*
12:10-12:30		Ahsan Javaid — *Prediction of Power Supply Induced Jitter via Deep Belief and Knowledge-based Neural Networks*
12:30-14:00		*Lunch*
14:00-14:20	SESSION 5 — Outreach and cross-disciplinary applications — Chair: Nikhita Baladari	Fábio Coutinho — *On the Performance Analysis of DL-based Data Detection Algorithms in M-QAM Satellite Links*
14:20-14:40		Mounir Abdkrimi — *Modeling and Analysis of Digital-to-Analog Converter Non-Idealities in Microwave Kinetic Inductance Detectors Readout*
14:40-15:00		Ricardo Lameirinhas — *High Sensitivity Sensors based on Slit Plasmonic Gold Nanoantennas*
15:00-15:20		Akira Tsuchiya — *Mean-Free-Path-Based Evaluation of Size Effect and Anomalous Skin Effect in On-Chip Interconnects under Cryogenic Environment*
15:20-15:50		*Coffee-Break*
15:50-17:20		INDUSTRY FORUM — Moderators: Stefano Grivet-Talocia and Christian Schuster
19:00 onwards		Gala Dinner

May 15, Wednesday

Time	Session	Event
09:30-09:50	SESSION 6 — Coupling characterization and reduction — Chair: Igor S. Stievano	Jose Schutt-Aine — *Signal and Power Integrity Co-Simulation of Chiplet-to-Chiplet Channel based on Latency Insertion Method*
09:50-10:10		Francesco de Paulis — *Time Domain Assessment of Minimum FEXT by Tabbed Line Design*
10:10-10:30		Alexander Gäbler — *Efficient Investigation of Coupled Lines in Quasi periodical High-density Signal Routings for HPC Applications*
10:30-11:00		*Coffee-Break*
11:00-11:10		SPONSOR PITCH — José Pedro Borrego — *ANACOM*
11:10-11:30	SESSION 7 — Electrical and electromagnetic performance analysis — Chair: Ivan Ndip	Jun-Bae Kim — *Analysis of the Effects of Power Partitioning in LPDDR4x Package for Enhanced EMC Design*
11:30-11:50		Ahmet C. Durgun — *Tree-based Sequential Sampling for Efficient Designs in Package Electrical Analysis*
11:50-12:10		Yanming Zhang — *Electromagnetic Near-Field Scanning with a Spatially Sparse Sampling Strategy Utilizing Kriging-DMD*
12:10-12:30		Closing Session
12:30-14:00		*Lunch*
14:00-18:00		IBIS SUMMIT — Chair: Markus Buecker

SPI 2024 - 28th IEEE Workshop on Signal and Power Integrity
May 12-15, 2024 -- Lisbon, PORTUGAL
E-mail: spi2024@av.it.pt | *Website:* spi2024.av.it.pt | *LinkedIn:* linkedin/spi2024

FINAL PROGRAM

TUTORIAL AND TECHNICAL SESSIONS

May 12, Sunday

15:00 – 17:30   **TUTORIAL**

Lorenzo Codecasa
Politecnico di Milano, Milan, Italy
Thermal Modeling of Electronic Components and Packages

May 13, Monday

09:50 – 10:30   **KEYNOTE**

Rajen Murugan
Texas Instruments, Inc., Dallas (TX), USA
Multiphysics and Multidomain Modeling of Semiconductor IC Packaging and Systems

SESSION 1
11:00 – 12:20   **POWER DISTRIBUTION NETWORKS**
Chair: Heidi Barnes

11:00
Judy Amanor-Boadu, E Hammond
Intel Corporation, USA
Leveraging SIMPLIS to Better Predict Server Platform Power Delivery Performance

11:20
Morten Schierholz (1), Zouhair Nezhi (2), Marcus Stiemer (2), Christian Schuster (1)
(1) Hamburg University of Technology, Germany; (2) Helmut Schmidt University, Germany
PCB based Power Deliver Network Analysis Using Transfer Learning and Artificial Neural Networks

11:40
Youcef Hassab, Morten Schierholz, Christian Schuster
Hamburg University of Technology, Germany
Application of Gaussian Process Regression for Data Efficient Prediction of PCB-based Power Delivery Network Impedance Features

12:00

Antonio Carlucci, <u>Tommaso Bradde</u>, Stefano Grivet-Talocia

Politecnico di Torino, Italy

Fast Prediction of Worst-Case Voltage Droops in Power Distribution Networks

14:00 – 14:40   **KEYNOTE**

<u>Cian Ó Mathúna</u>

Tyndall National Institute, University College Cork, Ireland

MagIC – Making Magnetics Disappear onto Silicon Enabling Power Supply on Chip (PwrSoC) and Power Supply in Package (PwrSiP)

SESSION 2
14:40 – 15:40   **MODELS AND METHODS FOR SI/PI ANALYSIS**
Chair: Jose Schutt-Aine

14:40

<u>Tim Pattyn</u>, Arno Moerman, Martijn Huynen, Dries Vande Ginste

Ghent University - imec, Belgium

Differential Interconnects with Integrated Equalization and Common-Mode Filtering for Broadband Signal Integrity Enhancement in High-Speed PAM-4 Signaling

15:00

<u>Marco Occhiali</u> (1), Aurora Sanna (2), Simona Cucchi (2)

(1) Ansys Italia, Italy; (2) STMicroelectronics, Italy

Impact of Port Type in S-Parameter Extraction of Package and PCB High-Speed Interconnections

15:20

Andrea Gaetano Chiariello (1), <u>Giulia Di Capua</u> (2), Antonio Maffucci (2), Nicola Femia (3)

(1) University of Campania, Italy; (2) University of Cassino and Southern Lazio, Italy; (3) University of Salerno, Italy

Models and Methods for the Analysis of PCB Crosstalk in Switch-Mode Power Supplies

15:50 – 16:50   **POSTER SESSION**
Chairs: Antonio Maffucci and Stefano Grivet-Talocia

P-01

<u>Jose Moreira</u> (1), Sergey Churkin (2), Margarita Kirillova (2)

(1) Advantest, Germany; (2) Radiogigabit, Armenia

A Dual-Polarized Quad-Ridged Waveguide Antenna for OTA Near-Field ATE Socket in 5G-FR2 band

P-02

Simona Cucchi, <u>Aurora Sanna</u>

STMicroelectronics, Italy

Advanced package decoupling study for power integrity optimization of high-end digital devices

P-03

Soazig Le Bihan (1), Tristan Dubois (2), Jean-Baptiste Begueret (2), Marc Gatti (1), Adil El Abbazi (1), Pierre Amblard (2)
(1) THALES Avionics, France; (2) IMS Bordeaux, France

Methodology for optimizing Ethernet links at 10 and 25Gbps for critical systems in the aerospace environment

P-04

Jose Enrique Hernandez-Bonilla (1), Golzar Alavi (1), Torsten Reuschel (2), Cheng Yang (3), Christian Schuster (3)
(1) Robert Bosch GmbH, Germany; (2) University of New Brunswick, Canada; (3) Hamburg University of Technology, Germany

Uncertainty Quantification of the Insertion Loss of an Automotive PCB Stripline

P-05

Gyeongchan Jang (1), Jiseong Kim (2), Hyun Ho Park (3), Eakhwan Song (4)
(1) Vatech, South Korea; (2) Korea Advanced Institute of Science and Technology, South Korea; (3) University of Suwon, South Korea; (4) Kwangwoon University, South Korea

Segmented Cavity Design for Suppression of Cavity-to-Via Coupling in High-Speed Transmission Lines of Multi-Layer Printed Circuit Boards

P-06

João Pinho Oliveira, Fábio Coutinho, Arnaldo Oliveira
Instituto de Telecomunicações, Universidade de Aveiro, Portugal

On the Performance Analysis of Automatic Gain Control Module in Quantized OFDM 5G Systems

P-07

Rahul Kumar, Manish Bansal
STMicroelectronics Pvt Ltd, India

Complete System Analysis of High Speed Serial Interfaces of data rate up to 20Gbps with IBIS-AMI Models

P-08

Hui Zhou
Ansys AB, Sweden

Automatic PCB Material Characterization Using Design of Experiments and Mixed-Integer Sequential Quadratic Programming

P-09

Nick K. H. Huang, Huai-De Tsai, Peng-Sheng Huang, Jim Lai
Hewlett Packard Enterprise, Taiwan

Validation of Switching Voltage Regulator Noise Mitigation to Signals

P-10

Jun Wang, Yan Xu, Haiyue Yuan, Yuhao Huang, Jianmin Lu, Xiuqin Chu
Xidian University, China

Analysis of Optimum Rotation Angle for Mitigating P/N Skew Based on Geometrical Method

P-11

Yuhao Huang, Tao Wei, Yuhuan Luo, Haiyue Yuan, Jun Wang, Xiuqin Chu
Xidian University, China

Analyzing Performance of Nonlinear High-Speed Links Based on Least Square Method

May 14, Tuesday

09:00 – 09:40   **KEYNOTE**

Kemal Aygün

Intel Corporation, Chandler (AZ), USA

Solving the Challenges of High-Speed/High-Bandwidth Interconnects for Future System-in-Packages

SESSION 3
10:50 – 12:30   **ELECTRO-THERMAL MODELING**
Chair: Joana Catarina Mendes

09:40

Sarah Sibilia (1), Francesco Siconolfi (1), Antonio Maffucci (1), Gaspare Giovinco (1), Isaac Appiah Otoo (2), Francesco Bertocchi (3), Sergio Chiodini (3)

(1) University of Cassino and Southern Lazio, Italy; (2) University of Eastern Finland, Finland; (3) Nanesa srl, Italy

Electro-thermal Response of Industrial-grade Graphene for Electronic Packages Applications

10:00

Lorenzo Codecasa (1), Vincenzo d'Alessandro (2), Antonio Pio Catalano (2), Ciro Scognamillo (2) Dario D'Amore (1)

(1) Politecnico di Milano, Italy; (2) University Federico II, Italy

Fast Error-Bounded MOR-based Approximation of Heat Conduction Problems in Electronics

SESSION 4
10:50 – 12:30   **AI-BASED APPROACHES FOR SI/PI ANALYSIS**
Chair: Kemal Aygün

10:50

Riccardo Trinchero (1), Tommaso Bradde (1), Mihai Telescu (2) Igor Simone Stievano (1)

(1) Politecnico di Torino, Italy; (2) Univ Brest, CNRS, France

Modeling of IC Buffers from Channel Responses via Machine Learning Kernel Regression

11:10

Jan Krummenauer (1), Alex Schuler (1), Andrew Ghaly (1), Juergen Goetze (2)

(1) Robert Bosch GmbH, Germany; (2) TU Dortmund, Germany

Evaluating Deep Reinforcement Learning for Macromodel Synthesis

11:30

Zouhair Nezhi (1), Marcus Stiemer (1), Morten Schierholz (2), Christian Schuster (2)

(1) Helmut Schmidt University, Germany; (2) Hamburg University of Technology, Germany

Dimensional Reduction by Auto-Encoders in Machine Learning Based Power Integrity Analysis

11:50

Yutaka Uematsu (1), Soshi Shimomura (1), Yasuhiro Ikeda (2)

(1) Hitachi, Ltd., Japan; (2) Hitachi Astemo, Ltd., Japan

Abnormal-state-clustering for In-vehicle Cable Communication using Equalizer Parameters and Machine Learning Approach

12:10

Ahsan Javaid (1), Ramachandra Achar (1), Jai Narayan Tripathi (2)

(1) Carleton University, Canada; (2) Indian Institute of Technology Jodhpur, India

Prediction of Power Supply Induced Jitter via Deep Belief and Knowledge-based Neural Networks

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SESSION 5

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14:00 – 15:20 **OUTREACH AND CROSS-DISCIPLINARY APPLICATIONS**

<div align="center">

Chair: Nikhita Baladari

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14:00

Fábio Coutinho (1), Hugerles Silva (1), Petia Georgieva (2), Arnaldo Oliveira (1)

(1) Instituto de Telecomunicações, Universidade de Aveiro, Portugal; (2) IEETA, Instituto de Telecomunicações, Universidade de Aveiro, Portugal

On the Performance Analysis of DL-based Data Detection Algorithms in M-QAM Satellite Links

14:20

Mounir Abdkrimi, Olivier Rossetto, Olivier Bourrion, Christophe Vescovi, Christophe Hoarau

Univ. Grenoble Alpes, CNRS, France

Modeling and Analysis of Digital-to-Analog Converter Non-Idealities in Microwave Kinetic Inductance Detectors Readout

14:40

Ricardo A. Marques Lameirinhas (1), João Paulo N. Torres (2), António Baptista (3), Maria João Marques Martins (4)

(1) Instituto de Telecomunicações & Instituto Superior Técnico, Portugal; (2) Instituto de Telecomunicações & Academia Militar, Portugal; (1) Instituto de Telecomunicações, Portugal; (4) Academia Militar, Portugal

High Sensitivity Sensors based on Slit Plasmonic Gold Nanoantennas

15:00

Akira Tsuchiya

The University of Shiga Prefecture, Japan

Mean-Free-Path-Based Evaluation of Size Effect and Anomalous Skin Effect in On-Chip Interconnects under Cryogenic Environment

15:50 – 17:20 **INDUSTRY FORUM**

<div align="center">

Moderators: Stefano Grivet-Talocia and Christian Schuster

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Kemal Aygün – *Intel Corporation, USA*

Heidi Barnes – *Keysight Technologies, USA*

Olivier Bayet – *STMicroelectronics, France*

Xiaomin Duan – *IBM, Germany*

Vaishnav Srinivas – *Qualcomm, USA*

May 15, Wednesday

SESSION 6

09:30 – 10:30   **COUPLING CHARACTERIZATION AND REDUCTION**
Chair: Igor S. Stievano

09:30

Yi Zhou, Bobi Shi, Thong Nguyen, Haofeng Sun, <u>Jose E. Schutt-Aine</u>
University of Illinois at Urbana-Champaign, USA
Signal and Power Integrity Co-Simulation of Chiplet-to-Chiplet Channel based on Latency Insertion Method

09:50

<u>Francesco de Paulis</u> (1), Carlo Olivieri (1), Alessandro Pali (2)
(1) University of L'Aquila, Italy; (2) SECO s.p.a., Italy
Time Domain Assessment of Minimum FEXT by Tabbed Line Design

10:10

<u>Alexander Gäbler</u> (1), Uwe Maass (1), Ivan Ndip (2)
(1) Fraunhofer IZM, Germany; (2) Fraunhofer IZM, Brandenburg University of Technology, Germany
Efficient Investigation of Coupled Lines in Quasi periodical High-density Signal Routings for HPC Applications

SESSION 7

11:10 – 12:10   **ELECTRICAL AND ELECTROMAGNETIC PERFORMANCE ANALYSIS**
Chair: Ivan Ndip

11:10

<u>Jun-Bae Kim</u>, Taeho Kim, Chang Soo Yoon, Janghoo Kim, Byungjin Kwon, Youngbong Han, Jungho Jin, Seungbae Lee, Yoo-Chang Sung, Seung-Jun Bae, Daihyun Lim, Tae-Young Oh
Samsung Electronics, South Korea
Analysis of the Effects of Power Partitioning in LPDDR4x Package for Enhanced EMC Design

11:30

Doğanay Özese (1), Mustafa Gökçe Baydoğan (1), <u>Ahmet C. Durgun</u> (2), Kemal Aygün (3)
(1) Boğaziçi University, Türkiye; (2) Middle East Technical University, Türkiye; (3) Intel Corporation, USA
Tree-based Sequential Sampling for Efficient Designs in Package Electrical Analysis

11:50

<u>Yanming Zhang</u> (1), Steven Gao (1), Lijun Jiang (2)
(1) Chinese University of Hong Kong, Hong Kong; (2) Missouri University of Science and Technology, USA
Electromagnetic Near-Field Scanning with a Spatially Sparse Sampling Strategy Utilizing Kriging-DMD

14:00 – 18:00   **IBIS SUMMIT**
Chair: Markus Buecker

Program to be announced